UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/527,422	03/17/2000	Alexander I. Krymski	08305-070001	4176

7590 11/16/2005

Micron Technology, Inc.
c/o Tom D'Amico
Dickstein, Shapiro, Moran & Oshinsky
2101 L Street, NW
Washington, DC 20037-1526

EXAMINER	
MISLEH, JUSTIN P	

ART UNIT	PAPER NUMBER
2612	

DATE MAILED: 11/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/527,422	KRYMSKI ET AL.	
	Examiner	Art Unit	
	Justin P. Misleh	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 6 and 8 - 40* is/are pending in the application.

4a) Of the above claim(s) *12 - 15 and 23 - 40* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 6, 9 - 11, 16 - 19, 21, and 22* is/are rejected.

7)☒ Claim(s) *8 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed August 24, 2005 have been fully considered but they are not persuasive.

2. Applicant argues, "Zhou et al. discloses ' ... sensing node 36 is clamped to VDD ...' ... The sensing node 36 is not equivalent to the 'pixel readout line' of claims 1, 16, and 22 ... there is no disclosure whatsoever in Zhou et al. to clamp a pixel output line to any voltage ..."

3. The Examiner respectfully disagrees with Applicant's position. As shown in figure 2 of Zhou et al., clamping the sensing node (36) to VDD would turn on the source follower transistor (42) such that VDD is passed through to the row select transistor (44). Zhou et al. states, in column 5 (lines 32 – 47), that during a reset operation a reset signal is applied to the reset transistor (38) such that the sensing node (36) becomes clamped to VDD. Furthermore, Zhou et al. also states, in column 5 (lines 48 – 61), that during a reset operation a row select signal is applied to the row select transistor (44) such that the column bus (16), which also corresponds to the "pixel readout line" (PXO), carries a voltage corresponding to VDD level of the clamped sensing node (36). Therefore, Applicant's statement "there is no disclosure whatsoever in Zhou et al. to clamp a pixel output line to any voltage" is completely erroneous.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. **Claims 1 – 6, 9 – 11, 16 – 19, 21, and 22** are rejected under 35 U.S.C. 102(e) as being anticipated by Zhou et al.

6. For **Claim 1**, Zhou et al. disclose, as shown in figures 1, 2, 5 and 7 and as stated in columns 4 (lines 37 – 47), 5 (lines 17 – 47), 9 (line 50) – 10 (line 20), a method of processing pixel levels, the method comprising:

clamping a pixel readout line (PXO) to a voltage level less than a voltage corresponding to a pixel signal (Figure 4 and column 7, lines 27 – 33, actually teach that reset level Vdd is less than the pixel signal. Specifically, PXO represents the pixel output line when it carries an image signal 101 and after it has been reset 103. Figure 4 clearly shows that the image signal is clamped to a lesser voltage value.);

subsequently coupling (via row select 44) the pixel readout line (PXO) to an output of an nMOS source-follower (42) and reading out the pixel signal onto the pixel readout line (PXO) through the nMOS source follow (42); and

storing a signal corresponding to the pixel signal that was read out (in capacitor 54).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing

diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

7. As for **Claim 2**, Zhou et al. disclose, as shown in figure 5 and 7, wherein clamping the pixel readout line (PXO) includes discharging a capacitance (74) on the pixel readout line (PXO). Sampling the reset level when SHR is high discharges the capacitor (74) coupled to the pixel read out line (PXO).

8. As for **Claim 3**, Zhou et al. disclose, as stated above, the reset level of a subsequent integration period is used with a previously stored sensed signal from a previous integration period and the CDS and clamping circuit 22 is a processing circuit. Therefore, Zhou et al. disclose wherein discharging the pixel readout line is performed while processing a previously-stored pixel signal.

9. As for **Claim 4**, Zhou et al. disclose wherein discharging the pixel read out (PXO) includes disabling a pixel selection switch (row select switch 44 is turned off when discharging capacitor 74, see timing diagram of figure 7).

10. As for **Claim 5**, Zhou et al. disclose wherein discharging the pixel read out including enabling a switch (123) to couple the pixel readout line to ground.

11. As for **Claim 6**, Zhou et al. disclose, clamping a capacitive storage node (54/74) in a pixel processing circuit (22; see above) to a voltage less than a voltage corresponding to the pixel signal appearing on the pixel readout line (PXO; 74 stores the reset level of the APS);

subsequently coupling the pixel readout line (PXO) to the storage node in the processing circuit (22; during a SHR high signal thereby sampling the reset of a subsequently integration period); and

storing the signal corresponding to the pixel signal on the capacitive storage node (54).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

12. As for **Claim 9**, Zhou et al. disclose resetting the pixel; subsequently reading out a reset signal through the nMOS (42) source-follower; and storing on a second capacitive storage bode

(54/74) in the processing circuit (22) a signal that corresponds to the reset signal (see below for explanation).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

13. As for **Claim 10**, Zhou et al. disclose, prior to storing the signal corresponding to the reset signal, clamping the second capacitive storage node (54/74) to a voltage less than the voltage corresponding to the reset signal; and subsequently coupling the pixel readout line (PXO) to the second storage node to store the signal corresponding to the reset signal on the second storage node.

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row

select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

14. As for **Claim 11**, Zhou et al. disclose, as shown in figure 5, that the processing circuit (22) includes a pMOS transistor (130/150) source-follower that the pixel signal is passed through.

15. For **Claim 16**, Zhou et al. disclose, as shown in figures 1, 2, 5 and 7 and as stated in columns 4 (lines 37 – 47), 5 (lines 17 – 47), 9 (line 50) – 10 (line 20), an imager comprising:

a pixel readout line (PXO);

an active pixel sensor (14) including an n-MOS source-follower (42) through which signals sensed by the sensor (34) can be read out to the pixel readout line (PXO), a first switch (44) that can be enabled to read signals from the sensor, and a reset switch (38);

a signal processing circuit that can be coupled to the pixel readout line (CDS and clamping circuit 22 coupled to PXO via connection 16); and

a controller (23) configured to provide control signals to cause the pixel read out line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor

and subsequently to cause the sensor signal to be read out through nMOS source follow (42) to the pixel read out line and to be stored (in capacitors 54 and 74) by the processing circuit (22; see explanation below).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

16. As for **Claim 17**, Zhou et al. disclose, as stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level

(reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

Therefore, Zhou et al. disclose wherein the controller is configured to provide a control signal to cause the first switch (44) to be disabled while a previously stored sensor signal (SHS) is being processed by the processing circuit (22).

17. As for **Claim 18**, Zhou et al. disclose, as shown in figure 5, a third switch (123) coupled between the pixel readout line (PXO) and ground, wherein the controller (23) is configured provide a control signal to cause the pixel readout line to be clamped by enabling the third switch (123).

18. As for **Claim 19**, Zhou et al. disclose, as shown in figure 5, wherein the processing circuit (22) includes a capacitive storage node (54 and 74), and wherein the controller (23) is configured to provide control signals (CSBB and CSB; see figure 5) to cause the capacitive storage node (54 and 74) to be clamped to a voltage less than a voltage corresponding to the sensor signal appearing on the pixel readout line (When CSBB is first turned on and CSB subsequently turned on charged stored on 54 and 74 are clamped down to VCM), and subsequently to cause the pixel readout line to be coupled to the storage node (In the subsequent sensed signal SHS period after said subsequent reset sampling period, the pixel readout line is again selected to be stored on the storage capacitor 54).

19. As for **Claim 21**, wherein the processing circuit includes a second capacitive node storage node (74), wherein the controller is configured to provide control signals to cause the reset switch in the pixel to be enabled, and subsequently to cause a resent signal to be read out on the pixel read out line through the nMOS (42) source-follower, and to cause a signal that corresponds to the reset signal to be on the second capacitive node (74).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. The CDS and clamping circuit 22 is a processing circuit since its operation is used for removing fixed pattern noises. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) to perform the processing.

20. For **Claim 22**, Zhou et al. disclose, as shown in figures 1, 2, 5 and 7 and as stated in columns 4 (lines 37 – 47), 5 (lines 17 – 47), 9 (line 50) – 10 (line 20), an imager comprising:

a pixel readout line (PXO);

an active pixel sensor (14) including an n-MOS source-follower (42) through which signals sensed by the sensor (34) can be read out to the pixel readout line (PXO), a first switch (44) that can be enabled to read signals from the sensor, and a reset switch (38);

a signal processing circuit (output processing circuit 25);

a pMOS source-follower (62 and 82; see figure 5) having an output that can be coupled to the processing circuit (25 via nodes 66 and 86) and

a controller (23) configured to provide control signals to cause the pixel read out line to be clamped to a voltage level less than a voltage corresponding to a signal sensed by the sensor and subsequently to cause the sensor signal to be read out through nMOS source follow (42) to the pixel read out line and to be passed to the processing circuit (25) through the pMOS source-follower (see explanation below).

As stated in column 5 (lines 33 – 47), first the APS is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by the sensor via reset transistor 38. Subsequently, the reset transistor 38 is turned off and the sensor 34 is integrated until a row select transistor 44 is turned on and the SHS (sample-and-hold signal) is high such that the integrated signal from the sensor 34 is sampled onto the capacitor 74 (as shown in the timing diagram of figure 7). After integration and sampling and while the row select is still turned on, the reset transistor 38 is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on the capacitor 54. Furthermore, it is important to note that Zhou et al. uses a previous sensed signal (that has been sampled and stored) and a reset level for a subsequent sensed signal (which is to be sampled and stored) in the CDS and clamping circuit includes pMOS source-followers 62 and 82 prior to outputting to the processing circuit 25.

Allowable Subject Matter

21. **Claims 8 and 20** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The following is a statement of reasons for the indication of allowable subject matter:

While the closest prior art teach an APS that is clamped (reset) to a voltage level less than a voltage corresponding to a signal sensed by a sensor via a reset transistor 38; subsequently, turning off the reset transistor integrating the sensor until a row select transistor is turned on and a SHS (sample-and-hold signal) is high such that the integrated signal from the sensor is sampled onto a capacitor; wherein after integration and sampling and while the row select is still turned on, the reset transistor is subsequently turned on such that clamped level (reset level) is sampled by a high SHR signal on to another capacitor.

However, the closest prior art does not teach or fairly suggest wherein a storage node is clamped to substantially the same voltage and at about the same time as a line for reading out the sensed signal from the APS (pixel readout line).

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

23. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Justin P Misleh whose telephone number is 571.272.7313. The Examiner can normally be reached on Monday through Friday from 8:00 AM to 5:00 PM.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Ngoc Yen Vu can be reached on 571.272.7320. The fax phone number for the organization where this application or proceeding is assigned is 571.273.3000.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JPM
November 12, 2005

NGOC-YEN VU
PRIMARY EXAMINER